Over operating free-air temperature range unless otherwise noted

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage range | 4.5 | 24 | V |
| $V_{INA-,INB-}$ | Input voltage range | -5 | 24 | |
| $T_J$ | Operating junction temperature | -40 | 150 | ℃ |

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1) | -2 | +2 | |

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$V_{IN}$=12V, $T_A$= 25℃.



Figure 1. UVLO vs Temperature



Figure 2. Supply current vs Temperature



Figure 3. Input Threshold vs Temperature



Figure 4. Enable Threshold vs Temperature



Figure 5 Output Rising Time vs Temperature

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Overview

The SCT52242 is a dual-channel non-invertible high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with the minimum propagation delay 13ns from input to output. The 1ns delay matching and the stackable output characteristics support higher driving capability demanding in high power converter applD 42/Lang (en-US)>> BDC q  0.00000912 0 612 792 r

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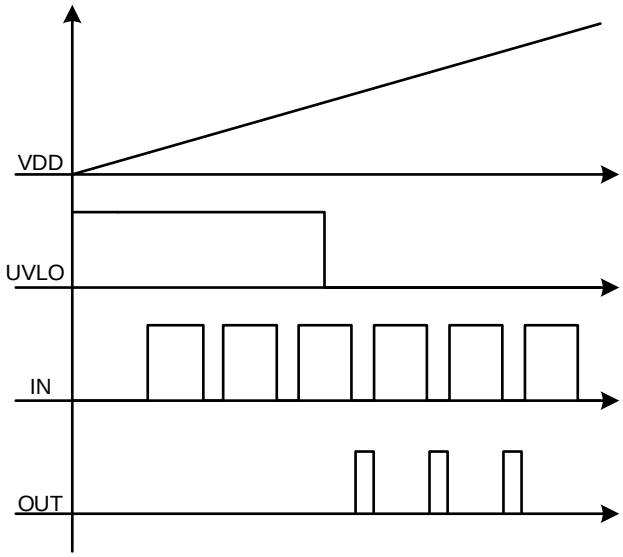


Figure 11. SCT52242 Output Vs VDD

Enable Function

SCT52242 provides independent enable pins ENA and ENB for external control of each channel operation. The enable pins are based on a TTL compatible input-threshold logic that is independent of the supply voltage and is effectively controlled with logic signals from 3V and 5V microcontrollers.

Figure 12. SCT52242 Output Stage

Stackable Output

The SCT52242 features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be stackable when the driven power device required higher driving capability. By using SCT52242, the OUTA and OUTB can be connected together to provide the higher driving capability, so does the INA- and INB-. As a result, a single input signal controls the stacked output combination. To support the stackable output, each channel output stage artificially implements up to 5ns dead-time to avoid the possible shoot-through between two channels as shown Figure 13.

Due to the rising and falling threshold mismatch between INA- and INB-, cautions must be taken when implementing stackable output of OUTA and OUTB together. The maximum mismatch between INA- and INB- input threshold is up to 10mV (maximum cross temperature), as a result the allowed minimum slew rate of input logic signal is 2V/us. The following suggestions are recommended when INA- and INB- connected together and along with the OUTA and OUTB:

1. Apply the fast slew rate dv/dt on input (2 V/us or greater) to avoid the possible shoot-through between OUTA and OUTB output stage.
2. INA- and INB- must be connected as close to the pins as possible.

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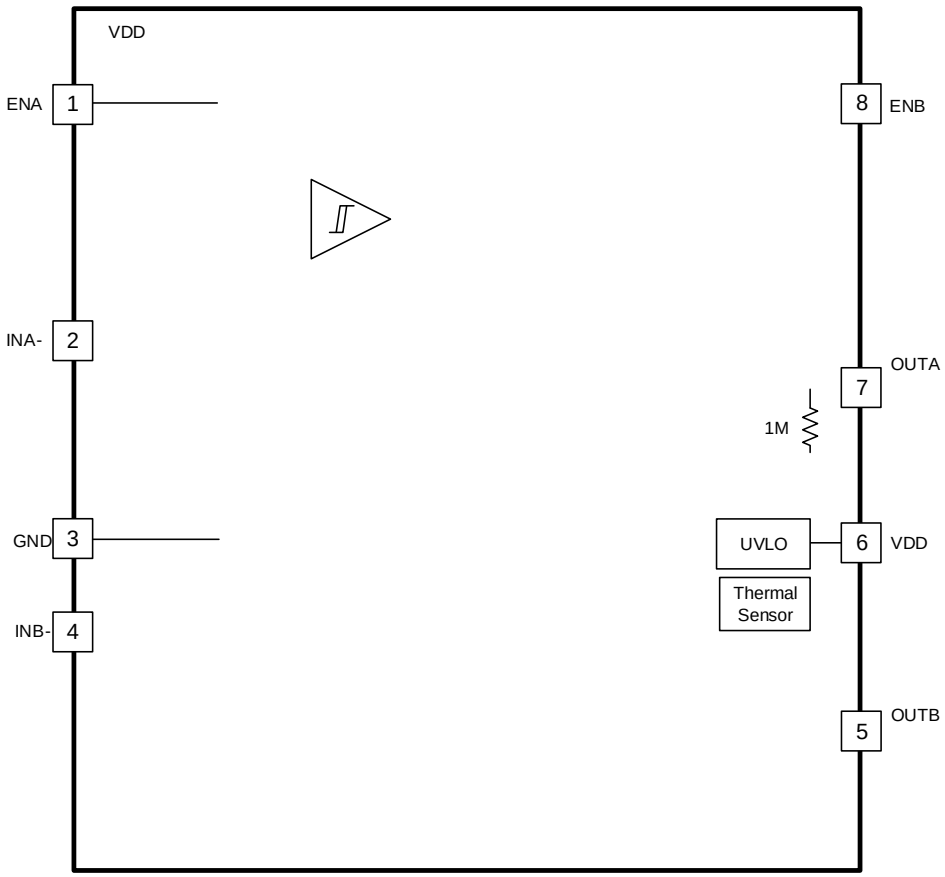


Figure 13. SCT52242 Stackable output

The Figure 14 and Figure 15 shows the stackable output with 2V/us input signal.

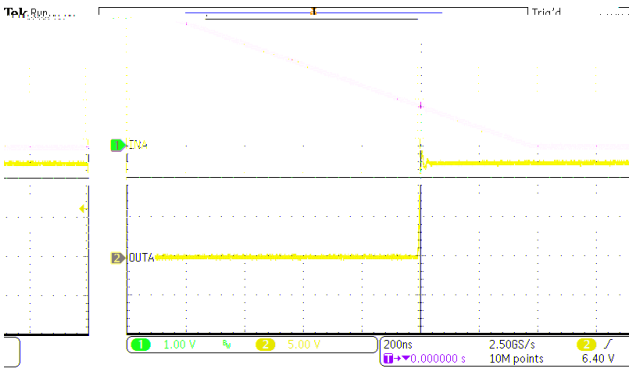


Figure 14. Driver Switching ON

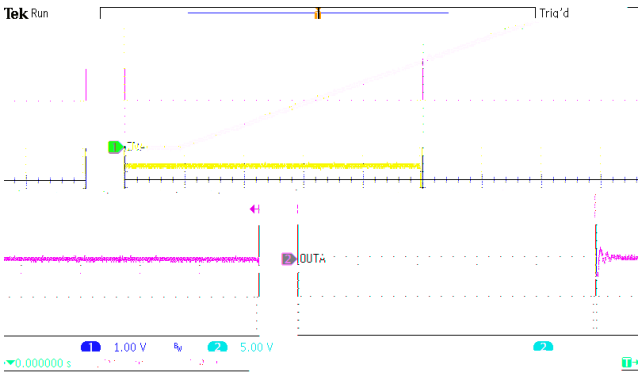


Figure 15. Driver Switching OFF

Thermal Shutdown

Once the junction temperature in the SCT52242 exceeds 170  C, the thermal sensing circuit stops switching until the junction temperature falling below 145  C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

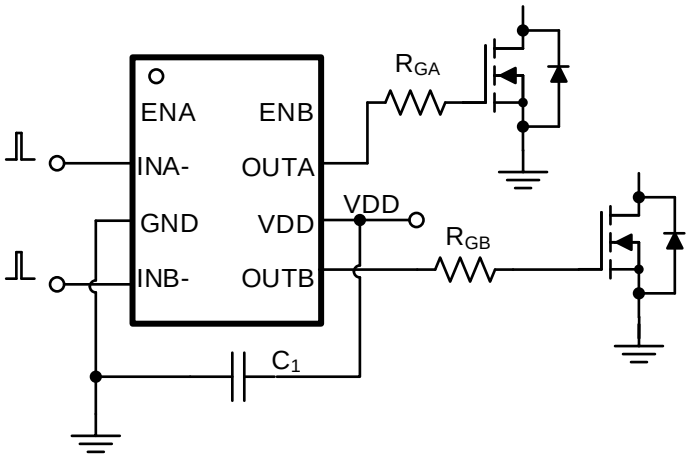


Figure 16. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52242 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52242 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52242 is:

(1)

Where

- $V_{DD}$ is supply voltage
- $C_{Load}$ is the output capacitance
- $F_{SW}$ is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52242 is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

(2)

Where

- $Q_g$ is the gate charge of the power device
- $f_{SW}$ is the switching frequency
- $V_{DD}$ is the supply voltage

If $R_G$ applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

(3)

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Where

- $R_{OH}$ is the equivalent pull up resistance of SCT52242
- $R_{OL}$ is the  pull down resistance of SCT52242
- $R_G$ is the gate resistance between driver output and gate of power device.

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## Application Waveforms

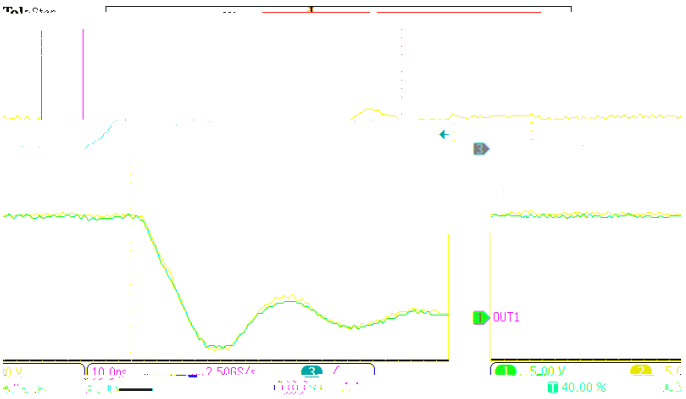


Figure 17. Driver Switching ON

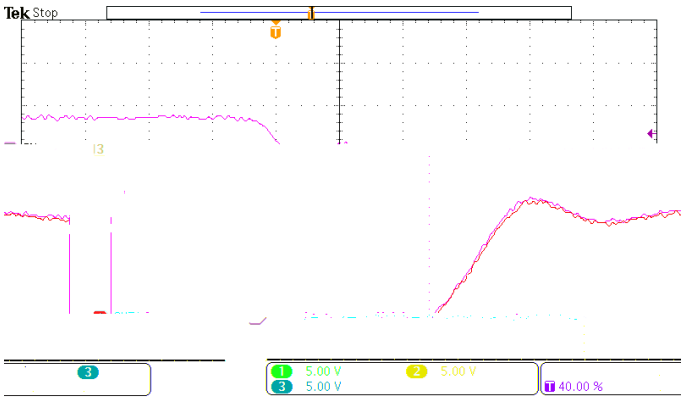


Figure 18. Driver Switching OFF

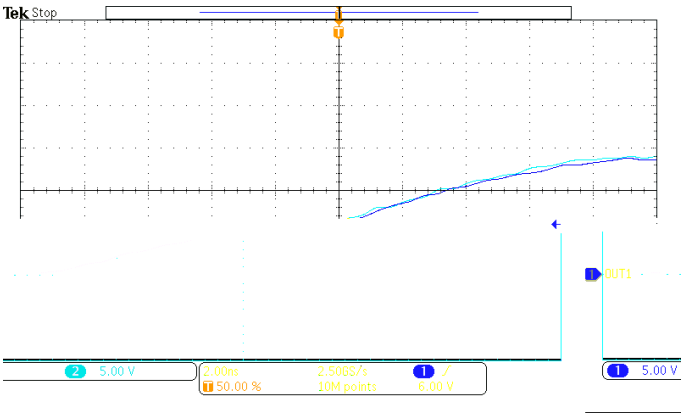


Figure 19. Delay Matching Rise

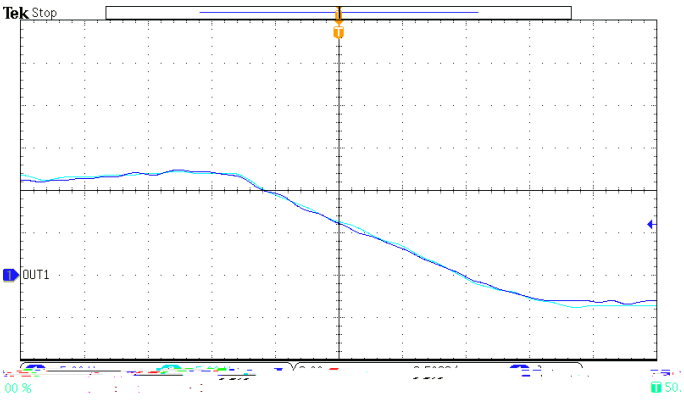


Figure 20. Delay Matching Fall

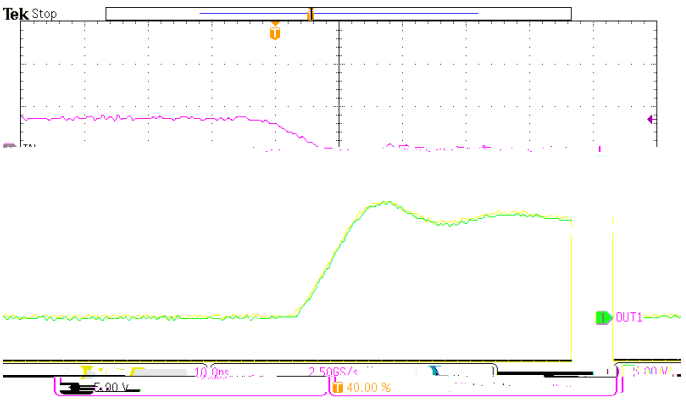


Figure 21. Stackable Output Rise

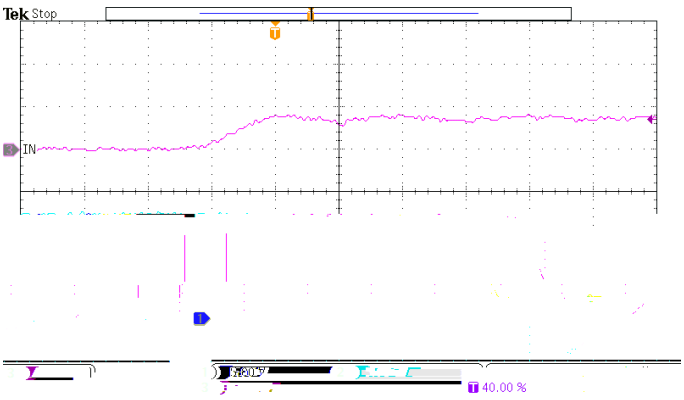


Figure 22. Stackable Output Fall

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Layout Guideline

The SCT52242 provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not designed well. The regulator could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. Below are the layout recommendations with using SCT52242 and Figure 23 is the layout example.

Put the SCT52242 as close as possible to the power device to minimize the gate driving loop including the driver output and power device gate. The power supply decoupling capacitors needs to be close to the VDD

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The real junction-to-ambient thermal resistance R $_{\theta JA}$ of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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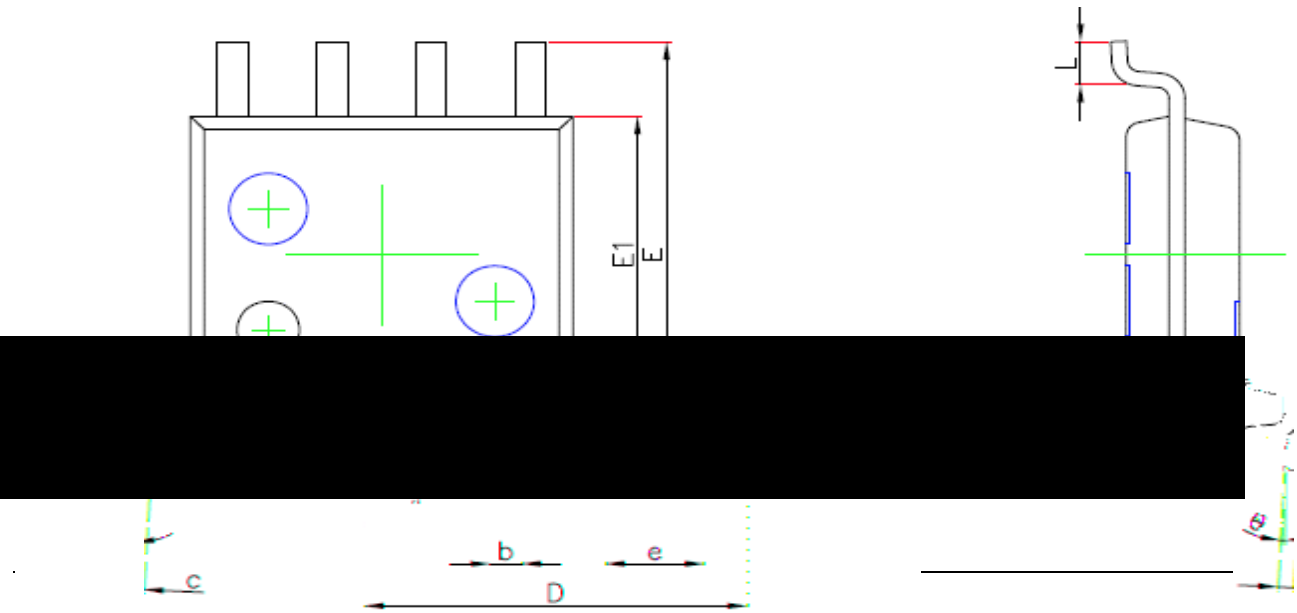


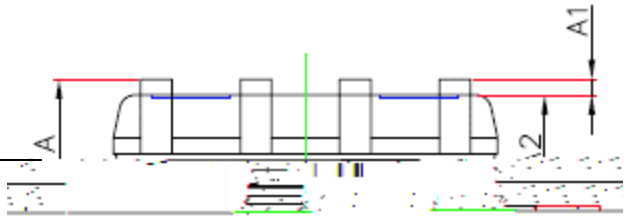




TOP VIEW




BOTTOM VIEW




SIDE VIEW

| SYMBOL | Unit: Millimeter | | |
|---|---|---|---|
| | MIN | TYP | MAX |

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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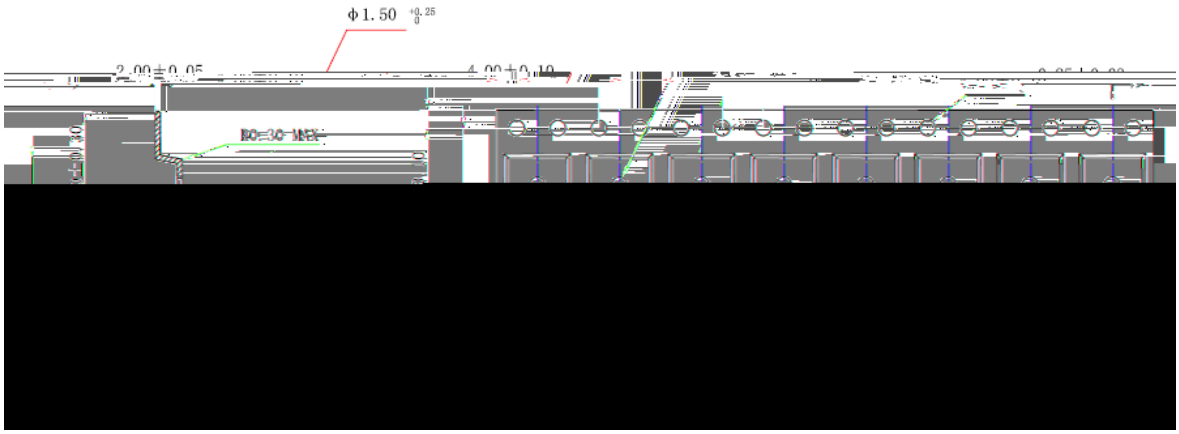

Feeding Direction

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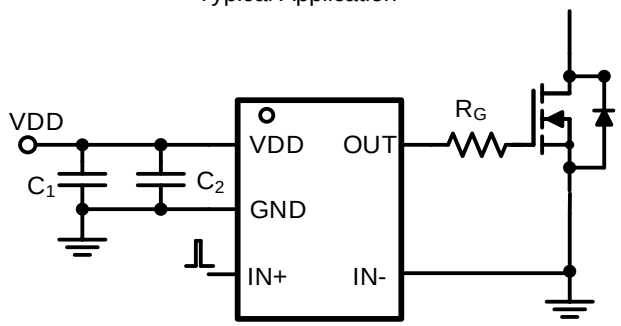
Single Channel, Non-Inverting MOSFET Gate Drive Typical Application




Typical Application Waveform

| PART NUMBERS | DESCRIPTION | COMMENTS |
|---|---|---|
| SCT51240 | Up to 24V Supply, 4-A Single Channel High Speed Low Side Driver | • Compatible for both Inverting and Non-inverting application<br>• Supporting down to -5V input |

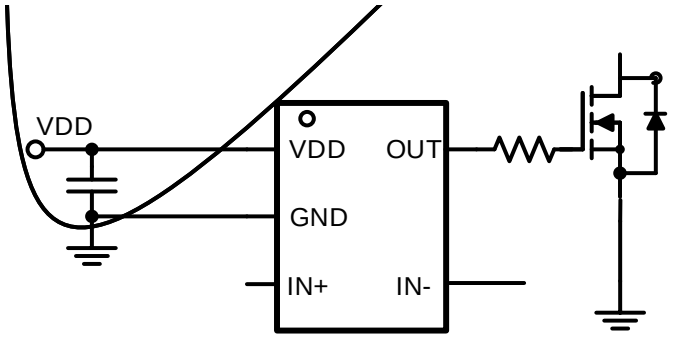



Figure 24. SCT51240 Inverting MOSFET Gate Drive Typical Application

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